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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/068,928	02/07/2002	Yee-Chia Yeo	2001-1379/24061.421	9422

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EXAMINER	
DOAN, THERESA T	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 12/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/068,928	YEO ET AL.	
	Examiner	Art Unit	
	Theresa T Doan	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *10/28/04* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. The Non-Final Rejection of the last Office action has been withdrawn. However, in view of further search, the new action has been made. This action is non-final rejection.

Claim Objections

2. Claim 22 is objected to because of the following informalities:

The limitations of "... a **strain** SiGe layer formed thereon, and a **relaxed** silicon layer formed on the SiGe layer" in lines 2-3 should be read "... a **relaxed** SiGe layer formed thereon, and a **strain** silicon layer formed on the SiGe layer". Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 and 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakaguchi et al. (6,221,738) as previously cited in view of Henley et al. (6,013,563).

Sakaguchi et al. teach in figures 4A-4D, a method of forming a strained semiconductor layer, comprising the steps of:

providing a first wafer (figure 4A) with a surface comprising of a first semiconductor layer 102 of a first natural lattice constant;

forming a second semiconductor layer 102 with a second natural lattice constant on the first semiconductor layer, a strain gradient would inherently introduce at the interface of the second semiconductor layer and the first semiconductor layer because of the bonding created at the interface;

providing a silicon second wafer 106 with a surface of an silicon dioxide insulator layer 105;

bonding the second semiconductor layer 102' on the surface of the second wafer 106, resulting in a third wafer (figure 4C) comprised of the second wafer 106, the second semiconductor layer 102', and the first wafer 101 (see figure 4C); and

performing an external force (column 25, lines 51-54) cleaving procedure at the strain gradient so that the second semiconductor layer 102' is separated from the first semiconductor layer 103 and the first wafer 101 (see figure 4D).

Sakaguchi does not disclose specific of performing an external force that can be used such as water jet.

Henley discloses a specific of performing an external force that can be used such as fluid jet (e.g, liquid jet or gas jet) or the compressed fluid source (e.g, pressurized liquid, pressurized gas) for separation layers (column 9, lines 29-52). Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the

invention was made to use fluid jet (e.g, liquid jet or gas jet) or the compressed fluid source (e.g, pressurized liquid, pressurized gas) as the external force for separating the layers in Sakaguchi's cleaving process because the fluid jet can be adjusted in direction, location, and magnitude to achieve the desired controlled cleaving process, as taught by Henley (column 9, lines 45-52).

5. Claims 1-4 and 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Godbey et al. (5,013,681) in view of Henley et al. (6,013,563).

Regarding claims 1-4 and 6-7, Godbey et al. teach in figures 9-12, a method of forming a strained semiconductor layer, comprising the steps of:

providing a first wafer (figure 9) with a surface comprising of a first SiGe semiconductor layer 72 of a first natural lattice constant (column 5, lines 39-50);

forming a second semiconductor layer 74 with a second natural lattice constant on the first semiconductor layer 72, a strain gradient would inherently introduce at the interface of the second semiconductor layer and the first semiconductor layer because of the bonding reacted at the interface;

providing a silicon second wafer (figure 10) with a surface of an SiO_2 insulator layer 82;

bonding the second semiconductor layer 74 on the surface of the second wafer, resulting in a third wafer (figure 11) comprised of the second wafer (handle wafer), the second semiconductor layer 74, and the first wafer (seed wafer) (see figure 11); and

performing a cleaving procedure so that the second semiconductor 74 is separated from the first semiconductor layer 72 and the first wafer.

Godbey et al. do not show performing a water jet cleaving procedure at the strain gradient to separate the second semiconductor layer from the first semiconductor layer and the first wafer.

Henley discloses performing fluid jet (e.g, liquid jet or gas jet) or the compressed fluid source (e.g, pressurized liquid, pressurized gas) for separation layers (column 9, lines 29-52). Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to use fluid jet (e.g, liquid jet or gas jet) or the compressed fluid source (e.g, pressurized liquid, pressurized gas) for separating the layers in Godbey's cleaving process because the fluid jet can be adjusted in direction, location, and magnitude to achieve the desired controlled cleaving process, as taught by Henley (column 9, lines 45-52).

Regarding claim 8, Godbey et al. teach in column 5, lines 39-50 and column 3, lines 45-56, the first semiconductor layer is an alloy semiconductor layer comprising of silicon and germanium, epitaxially grown to a thickness between about 0.1 to 10 microns, with a Ge mole fraction between about 5 to 80%.

Regarding claim 9, Godbey et al. teach the second semiconductor alloy layer is a silicon layer under tensile strain (column 4, lines 45-54).

Regarding claim 10, Godbey et al. teach the second semiconductor layer is a silicon layer, epitaxially grown to a thickness between about 20 to 1000 Angstroms (column 3, lines 60-62).

6. Claims 11-13 and 15-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sharma et al. (5,344,524) in view of Henley et al. (6,013,563).

Regarding claims 11-13 and 20-21, Sharma et al. teach in figure 5, a method of fabricating a metal oxide semiconductor field effect transistor (MOSFET) device on an insulator layer 22, featuring a silicon channel region 21, comprising the steps of:

providing a first wafer 20 with a surface comprising of a first semiconductor material 23 of a first natural lattice constant;

forming a second semiconductor layer 21 with a second natural lattice constant on the first semiconductor material so that the second semiconductor layer is strained and a large strain gradient would inherently form at the interface of the second semiconductor layer and the first semiconductor layer because of the bonding reacted at the interface;

providing a second silicon wafer 18 comprising of a substrate with an overlying SiO_2 insulator layer 22 (column 3, lines 67-68 and column 4, line 5);

bonding the second semiconductor layer 21 on the second wafer 18, with the insulator 22 in between, resulting in a third wafer comprised of the second wafer 18, the second semiconductor layer 21, and the first wafer 20;

performing a cleaving procedure so that the second semiconductor layer 21 is

separated from the first semiconductor material 23, resulting in a fourth wafer comprised of the second semiconductor layer 21 and the second wafer 18; and

forming a MOSFET device on the fourth wafer, comprising of a gate structure and of source and drain regions located adjacent to the gate structure.

Sharma et al. do not show performing a compressed air or pressurized fluid cleaving procedure at the strain gradient to separate the desire's layers.

Henley discloses performing the fluid jet (e.g, liquid jet or gas jet) or the compressed fluid source (e.g, pressurized liquid, pressurized gas) for separation process layers (column 9, lines 29-52). Accordingly, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to use the compressed fluid source (e.g, pressurized liquid, pressurized gas) for separating the layers in Sharma's cleaving process because the fluid jet can be adjusted in direction, location, and magnitude to achieve the desired controlled cleaving process, as taught by Henley (column 9, lines 45-52).

Regarding claims 15-17, Sharma et al. teach the first semiconductor material 23 is an alloy semiconductor layer comprising of silicon and germanium in a relaxed state wherein the alloy semiconductor layer 23 is epitaxially grown to a thickness between about 2 microns, with a Ge mote fraction between about 10% (column 3, lines 49-66 and column 4, lines 44-62).

Regarding claims 18-19, Sharma et al. teach the second semiconductor layer 21 is a silicon layer wherein the silicon layer is epitaxially grown to a thickness between about 0.01-2 microns (column 4, lines 22-30).

Regarding claims 22-23, Sharma et al. disclose a first wafer comprises a silicon substrate 20, a relaxed SiGe layer 23 formed thereon, and a strained silicon layer 21 formed on the SiGe layer (column 4, lines 40-52).

7. Claims 5 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakaguchi et al AND HENDLEY OR Godbey et al. and Henley et al. OR Sharma et al. and Henley et al. as applied to claims 3, 12 and further in view of King et al. (4,142,925) as previously cited.

Sakaguchi, Godbey and Sharma teach the insulator layer is a silicon dioxide layer but does not teach an insulator layer is a silicon nitride layer.

However, King et al. in column 2, lines 45-49, teach an insulator layer can be made of others suitable layer such as a silicon nitride layer for the well known purpose of protecting the silicon layer from the contaminants. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form an insulator layer is a silicon nitride layer in Sakaguchi, Godbey and Sharma's devices as set forth above because as taught by King, such a silicon nitride layer would protect the silicon layer from the contaminants.

Response to Arguments

Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday to Friday from 7:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-1562.

TD
December 1, 2004.

PHAT X. CAO
PRIMARY EXAMINER